

Sheet 2 of 9

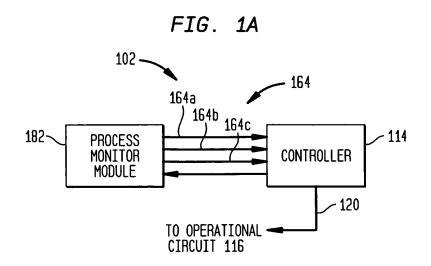
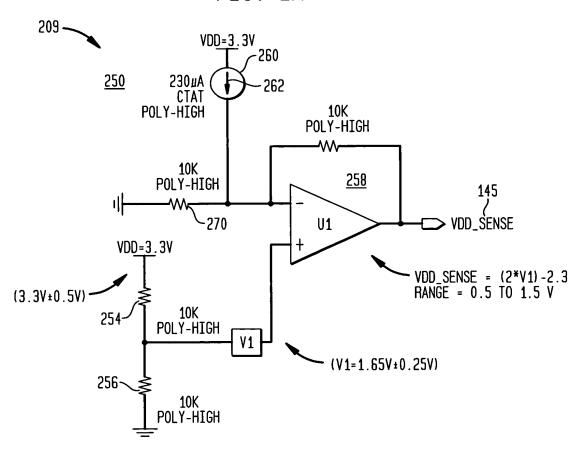
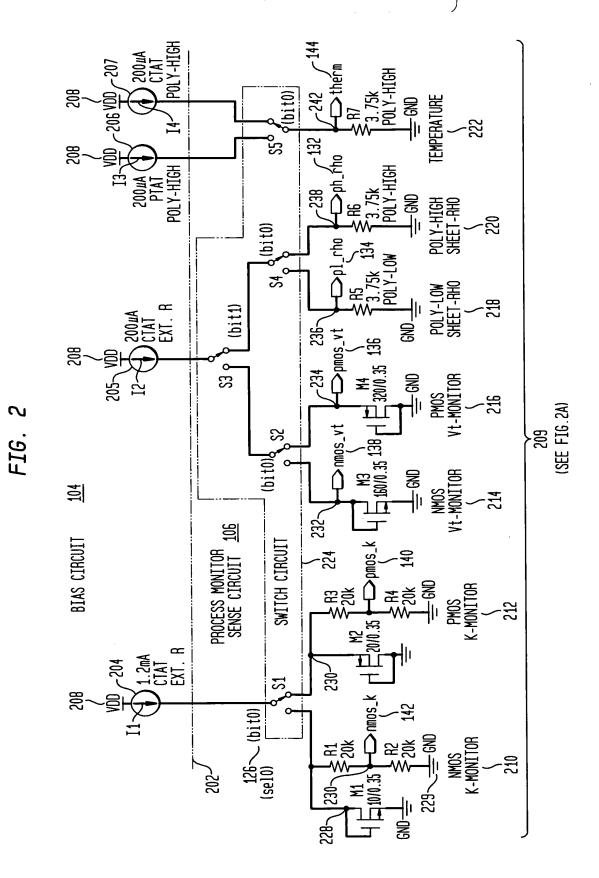


FIG. 2A

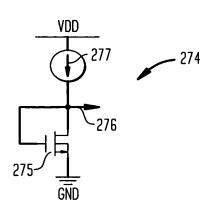


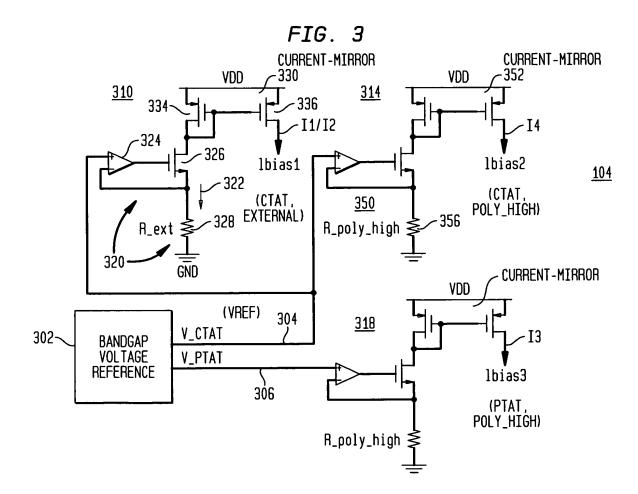
Appl. No. 10/647,472; Filed: August 26, 2003 Dkt. No. 1875.3770001; Group Art Unit: 2829 Inventors: Burns et al.; Tel: 202/371-2600 Title: Process Monitor For Monitoring An Integrated Circuit Chip



Sheet 4 of 9

FIG. 2B





R10 \geqslant R11 \geqslant 404 (V_CTAT) 304 (V_CTAT) 304 VREF \geqslant VREF \geqslant VREF \geqslant VREF \geqslant SUBSTRATE PNP's

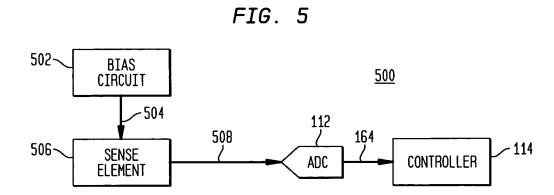
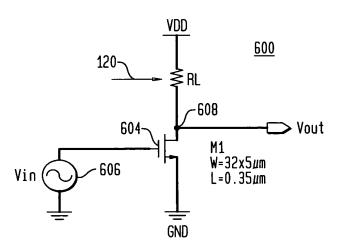
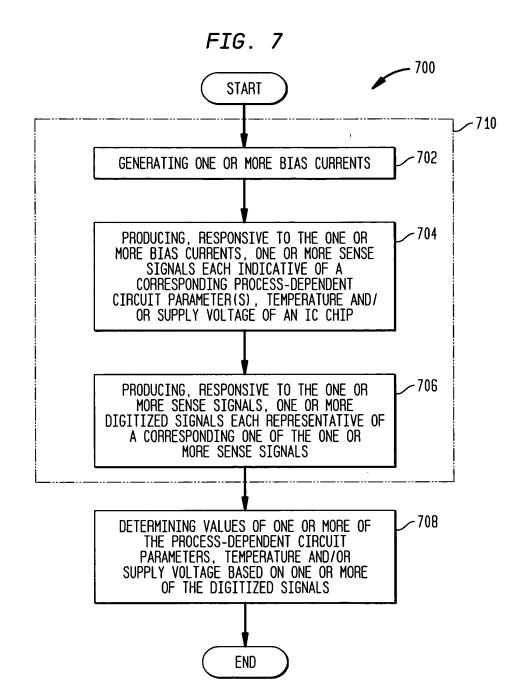
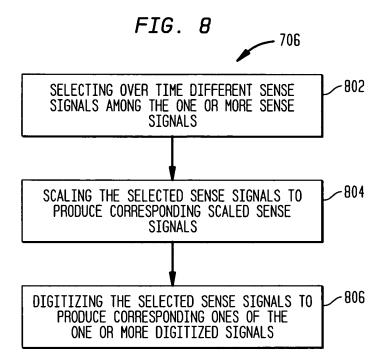
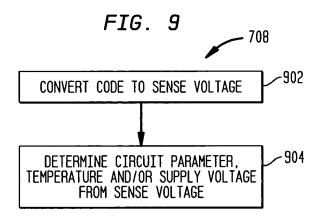


FIG. 6 OPERATIONAL CIRCUIT









Sheet 9 of 9



